Description

MEMORY DEVICE WITH PROGRAMMABLE RECEIVERS TO IMPROVE PERFORMANCE

BACKGROUND OF INVENTION

[0001] Technical Field

[0002] The present invention relates generally to the field of computer memory and more particularly, to multiple synchronous dynamic random access memory (DRAM) systems requiring faster performance.

[0003] Background

[0004] In recent years, the free fall of processor cycle times to levels well below access times of most dynamic random access memories has generated extensive research and development, the result of which has been the development of several generations of synchronous memory devices. Virtually all previously available semiconductor dynamic random access memory (DRAM) and many static random access memory (SRAM) devices used asyn-

chronous clocking systems in that the clocking signals necessary to perform memory access functions are not synchronized to the associated system processor. Although memories were accessed by signals sent by the processor, the exact time interval between the time a request was sent to a memory and the time a response was received was dependent on the particular internal features of the memory. Thus, it was necessary for system designers to allow for the "worst case" response time between requests for information and the anticipated time the information was available, which necessarily wasted time in the handling of many memory functions.

[0005] Improvements in semiconductor processing technology has enabled logic components such as microprocessors to operate at clock rates in excess of 3 GHz. Memory system clock rates have not kept pace because of the nature of DRAM memory devices . In order to perform well with these higher speed processors, synchronous dynamic random access memories (SDRAMs), operable with clock rates of up to 266 MHz. and data rates of up to 533 M Bits per second, have been designed. SDRAMs are responsive to a high frequency clock signal generated by the system clocking circuitry often running at a clock multiple versus

the processor, which renders all internal activity within the memory "synchronous" with other devices responsive to the same (or related) clock signal(s). In the synchronous approach, all SDRAM address and control inputs are sampled at the positive edge of the input clock, and all SDRAM outputs on recent DDR (Double Data Rate) SDRAMs are valid on subsequent positive and negative edges. This technique permits input/output transactions to take place on every clock cycle. SDRAMs can simplify both the overall system design and the memory-management subsystem, because the main memory operates in a deterministic, synchronous nature relative to the system clock.

[0006] As frequencies increase and cycle times decrease, memory designers are looking for additional ways to improve memory performance and timing margins. One element that can be improved is the timing adder due to the simultaneous switch affect of all the drivers to the SDRAMs switching in the same direction at the same time. This delay contribution is known as simultaneous switch (tSS). In recent low cost designs, this delay adder for tSS was as much as 1.06ns. This contribution was 14% of the total timing budget for a memory subsystem running at a 7.5ns cycle time.

[0007] Solutions to reduce the simultaneous switch delay adder include higher priced packaging, splitting the function across several components or running the memory at an increased cycle time.

[0008] Increased number of address/command signals due to larger DRAM or module densities only add to the simultaneous switch timing delays for high performance/low cost memory solutions. The price tag for two single 14 bit 1:2 registers is usually less than about $2.00.

[0009] Furthermore, the concept of driving buses with half of the drivers providing non-inverting polarities and the other half of the drivers providing inverted polarities is a known way of reducing simultaneous switch affects. But this technique does not cover devices receiving those signals to accept the inverted signal polarity and still function as if they received the non-inverted signal polarity.

[0010] Further, synchronous memory devices do not include the ability to be programmed to accept non- inverted or inverted address/command signals, so this technique has not previously been viable .

SUMMARY OF INVENTION

[0011] As clock frequencies increase and the cycle times decrease, the timing delay contribution of simultaneous

switching noise on the address/command bus, in a memory subsystem, is undergoing greater scrutiny. To achieve the emerging system memory performance targets (up to 500MHz clock speeds on multi-drop buses), new designs are required to ensure robust operation of the memory subsystem, without also incurring significant reductions in the system memory device count.

[0012] Further, as clock frequencies increase, the delay contribution of simultaneous switching push out on the address and command bus, in a memory subsystem, is becoming a major detractor. The present invention is directed to reduce the timing adder due to the drivers (which interface to the memory) switching all at the same time, in the same direction, thus allowing the memory system to meet faster performance and/or providing greater timing margin. This is accomplished by the use of drivers interfacing to the memory which provides both non-inverted and inverted address/command polarities to the SDRAMs. The SDRAMs have the capability to accept either non-inverted or inverted address/command polarities.

[0013] An example of the simultaneous switch impact is evident in the timing analysis (known as post-register timing analysis) on a Double Data Rate (DDR) SDRAM Registered

DIMM (Dual Inline Memory Module), which consists of DDR SDRAMs, a PLL for clock distribution on the module and one or more registers that latch and re-drive the address and command signals from the system memory controller to the SDRAMs (Synchronous DRAMs). The simultaneous switch push-out due to the drivers internal to the register switching at the same time has been as large as 700ps at a cycle time of 10ns (JEDEC Standard PC100 Registered DIMM). With current designs, the simultaneous switch push-out has been reduced to approximately 300ps at a cycle time of 3.75ns, but this continues to be approximately 7-8% of the timing budget. This simultaneous switch noise could be reduced by improving the register package, by further splitting the register function across multiple devices, or by reducing the memory load, and each has been leveraged to the acceptable cost/performance limit for the current technology. The present invention provides an alternate solution, whereby the DRAM itself is designed to operate with non-inverted or inverted address and command inputs.

[0014] Since many current (and most future) multi-drop memory subsystems will include pipelined address and command inputs (with these signals re-driven close to the DRAMs),

it is viable to design a memory device and memory subsystem to accommodate non-inverted and inverted address and command inputs to the DRAM. Also, since most high speed memory re-drive circuits will include multiple address/command outputs for a given input (for example, current and planned DDR DIMMs use 1:2 registers), the register can be designed to generate both non-inverted and inverted copies of the inputs (one each per input). This feature could be enabled, for example, via an external programming pin. Since SDRAMs are sensitive to the polarity of the address and commands for device programming and certain decoded operations, the memory devices would also require programming (such as via an external pin) to properly function with inverted inputs. The latter could easily be accomplished by either inverting or not the address and commands on the DRAM device, after the input receivers. In both the case of the DRAM and the register(s), the programming pin can be tied to ground to accept one polarity and tied to Vdd to accept the opposite polarity – thus always ensuring the correct signal polarity internal to the DRAM.

[0015] Although the embodiment described is in the context of a memory module (DIMM), this invention is not limited to

memory modules which include registers. Using this method, the simultaneous switch noise can be reduced in any memory subsystem which includes sufficient signals that simultaneous switch has a measurable affect on overall bus performance. It can also be expanded to include situations where only half of the memory address and control signals are inverted, or only the address signals are inverted, or only the command signals are inverted, or any other combination.

[0016] It should also be understood that increased package density and/or reductions in the area allocated to the memory subsystem will result in increased simultaneous switch affects, as more outputs on less packages will be switching, and current methods will not serve to decrease the number and combinations of outputs switching at a given time. The proposed solution may provide only a small benefit (10-20%) in applications with several re-drive devices, but a very sizeable benefit (50% or greater) in applications with a single re-drive device and a large number of inputs and outputs. Current plans for DDR II server memory subsystems include low-cost registers with 28 inputs and 2 to 3 output copies.

[0017] It is therefore an object of the present invention to pro-

vide a significant benefit to the post-register timing.

[0018] Another object is to obtain maximum operating clock speed for the memory subsystem.

[0019] These and other objects, advantages and features of the present invention will be more readily understood from the following detailed description of certain preferred embodiments of the invention.

BRIEF DESCRIPTION OF DRAWINGS

[0020] FIG. 1 is a block diagram of a DIMM designed in accordance with the present invention.

DETAILED DESCRIPTION

[0021] A memory module in accordance with the present invention contains multiple synchronous memories which are physically similar and architecturally compatible with a conventional memory module containing multiple asynchronous memories. For purposes of explanation the implementation of the invention utilizes a dual in-line memory module (DIMM) containing multiple synchronous memories. However, the invention is equally applicable to single in-line memory modules (SIMMs), and other arrangements in keeping with the spirit of the invention. Along with the advantage of compatibility, a memory

module of synchronous memory in accordance with the present invention preferably employs special placement and wiring of decoupling capacitors about the synchronous memories to reduce simultaneous switching noise during read and write operations.

[0022] Attention is directed to FIG. 1 which illustrates the use of the present invention in a DIMM module using a register and DRAM with inverted address/command (A/C) nets. A plurality of DRAMs 10 are arranged on a DIMM module. A register 11 is shown receiving inputs to the DIMM from a memory controller not shown for each DRAM (D, . . . Dn) along with an inverted B input which is tied to Vdd . The register 11 is programmed to provide non-inverted address/command inputs (+A/C) and inverted inputs (-A/C) to selected DRAMs 10. The selected DRAMs 10 accept either a +A/C or a -A/C signal based on the polarity of the program pin A/C on each DRAM which is tied to Vdd for non-inverting inputs and to Gnd (ground) for inverted inputs.

[0023] The simplest implementation of this invention is to use programmable pins on both the register and DRAM. These program pins are hardwired by design on the DIMM module and therefore transparent to the system. Another im-

plementation option is to have this programmability built into the DRAM and register or memory controller via programmable registers. This is more complex and would require the memory controller/processor to interrogate the devices to see if this option is on the devices during the initialization as well as the DRAMs and memory controller or register coming up in a default state (all non-inverted). Then the memory controller would then program the devices to either stay as non-inverted or change to inverted. This programming can be done by writing a register in the devices via a special command on the existing bus or could be done in parallel via a separate bus such as an I2C serial bus or JTAG bus.

[0024] As mentioned above, conventional methods for reducing simultaneous switch noise included: improving the power and ground distribution within the package (adding cost and increasing device and card wiring complexity); slowing down the drivers that are driving the signals to the DRAMs (which impacts performance); reducing the number of drivers per component (adding cost and requiring additional space); and reducing the re- driven signal count (by reducing the component density). It should be realized that the subject invention provides the greatest

benefit at the lowest cost.

[0025] Others have had to go with more complex and expensive packaging to reduce the simultaneous noise, or have used additional components to spread the function across multiple devices. The present invention reduces the maximum count of drivers that will be switching in anyone direction at a time, by utilizing a memory device that is designed to accept inverted inputs when so programmed. This invention will not add complexity or cost to either part, and the performance benefit gained will exceed the minimal delay impact that might occur in the memory or register device. In addition, this design decreases the min/max timing variation (spread) for all possible output signal combinations, thereby increasing the valid window of time for these signals at the receiving device. Independent of all other factors, increasing the valid window for these signals will permit higher frequency operation.

[0026] While the invention has been described in detail herein in accordance with certain preferred embodiments thereof, many modifications and changes therein may be effected by those skilled in the art. Accordingly, it is intended by the appended claims to cover all such modifications and changes as fall within the true spirit and scope of the in-

vention.